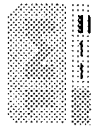


Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4396	(scan adj2 test\$3)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:17
L2	87	(scan adj2 test\$3) and edge-triggered	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:18
L3	85	(scan adj2 test\$3) and edge-trigger\$3 and (flip-flop\$1 or latch\$3)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:18
L4	21	(scan adj2 test\$3) and (edge-trigger\$3 or (edge adj2 trigger\$3)) and (flip-flop\$1 or latch\$3) and (combinatorial adj2 logic)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:20
L5	16	(scan adj2 test\$3) and (edge-trigger\$3 or (edge adj2 trigger\$3)) and (flip-flop\$1 or latch\$3) and (combinatorial adj2 logic) and (multiplex\$3)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:20
L6	20	(scan adj2 test\$3) and (edge-trigger\$3 or (edge adj2 trigger\$3)) and (flip-flop\$1 or latch\$3) and (combinatorial adj2 logic) and (multiplex\$3 or select\$3)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:21
L7	22	(scan adj2 test\$3) and (first adj2 domain\$1) and (second adj2 domain\$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:22
L8	19	(scan adj2 test\$3) and (first adj2 clock adj2 domain\$1) and (second adj2 clock adj2 domain\$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:22
L9	57	(first adj2 clock adj2 domain\$1) and (second adj2 clock adj2 domain\$1) and test\$4	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:23
L10	8	(first adj2 clock adj2 domain\$1) and (second adj2 clock adj2 domain\$1) and test\$4 and (edge-trigger\$4 or (edge adj2 trigger\$4))	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:23
L11	8	(first adj2 clock adj2 domain\$1) and (second adj2 clock adj2 domain\$1) and test\$4 and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:27

L12	54	(clock adj2 domain\$1) and test\$4 and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:27
L13	13	(clock adj2 domain\$1) and (scan adj2 test\$4) and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:28
L14	10	(clock adj2 domain\$1) and (scan adj2 test\$4) and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1) and (select\$4 or multiplex\$4)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:29
L15	0	(plurality adj3 clock adj2 domain\$1) and (scan adj2 test\$4) and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1) and (select\$4 or multiplex\$4)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:30
L16	8	(clock adj2 domain\$1) and (scan adj2 test\$4) and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1) and (select\$4 or multiplex\$4) and (test adj2 mode)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:31
L17	5	(clock adj2 domain\$1) and (scan adj2 test\$4) and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1) and (select\$4 or multiplex\$4) and (test adj2 mode) and TDI and TDO and TCK	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:33
L18	40	(clock adj2 domain\$1) and (latch\$4 or flip-flop\$1) and (select\$4 or multiplex\$4) and (test adj2 mode) and TDI and TDO and TCK	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:34
L19	30	(clock adj2 domains) and (latch\$4 or flip-flop\$1) and (test adj2 mode) and TDI and TDO and TCK	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:35
L20	30	(clock adj2 domains) and (latch\$4 or flip-flop\$1) and (test adj2 mode) and TDI and TDO and TCK	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:36

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE


[Membership](#) [Publications/Services](#) [Standards](#) [Conferences](#) [Careers/Jobs](#)
**IEEE Xplore**  
RELEASE 1.8

 Welcome  
 United States Patent and Trademark Office


» See

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)
**Welcome to IEEE Xplore**

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

**Tables of Contents**

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

**Search**

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

**Member Services**

- ☐ Join IEEE
- ☒ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

**IEEE ACCOUNTS**

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

 Your search matched **5** of **1094442** documents.

 A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

**Refine This Search:**

You may refine your search by editing the current search expression or entering new one in the text box.


☐ Check to search within this result set

**Results Key:**
**JNL** = Journal or Magazine    **CNF** = Conference    **STD** = Standard

**1 High-frequency, at-speed scan testing**

*Xijiang Lin; Press, R.; Rajski, J.; Reuter, P.; Rinderknecht, T.; Swanson, B.; Tamarapalli, N.;*  
 Design & Test of Computers, IEEE , Volume: 20 , Issue: 5 , Sept.-Oct. 2003  
 Pages:17 - 25

[\[Abstract\]](#)   [\[PDF Full-Text \(292 KB\)\]](#)   **IEEE JNL**
**2 System issues in boundary-scan board test**

*Parker, K.P.;*  
 Test Conference, 2000. Proceedings. International , 3-5 Oct. 2000  
 Pages:724 - 728

[\[Abstract\]](#)   [\[PDF Full-Text \(308 KB\)\]](#)   **IEEE CNF**
**3 Scan test data volume reduction in multi-clocked designs with safe capture technique**

*Jain, V.; Waicukauski, J.;*  
 Test Conference, 2002. Proceedings. International , 7-10 Oct. 2002  
 Pages:148 - 153

[\[Abstract\]](#)   [\[PDF Full-Text \(439 KB\)\]](#)   **IEEE CNF**
**4 The testability features of the 3rd generation ColdFire<sup>(R)</sup> family of microprocessors**

*Crouch, A.L.; Mateja, M.; McLaurin, T.L.; Potter, J.C.; Tran, D.;*  
 Test Conference, 1999. Proceedings. International , 28-30 Sept. 1999  
 Pages:913 - 922

[\[Abstract\]](#)   [\[PDF Full-Text \(800 KB\)\]](#)   **IEEE CNF**

---

**5 Advanced synchronous scan test methodology for multi clock domain ASICs***Schmid, J.; Knablein, J.;*

VLSI Test Symposium, 1999. Proceedings. 17th IEEE , 25-29 April 1999

Pages:106 - 113

[\[Abstract\]](#)[\[PDF Full-Text \(248 KB\)\]](#)**IEEE CNF**

---

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) |  
[New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online](#)  
[Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE


[Membership](#) [Publications/Services](#) [Standards](#) [Conferences](#) [Careers/Jobs](#)
**IEEE Xplore**  
RELEASE 1.8

 Welcome  
 United States Patent and Trademark Office


» See

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)
**Welcome to IEEE Xplore**

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

**Tables of Contents**

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

**Search**

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

**Member Services**

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

**IEEE Enterprise**

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

 Your search matched **30** of **1094442** documents.

 A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

**Refine This Search:**

You may refine your search by editing the current search expression or entering new one in the text box.


☐ Check to search within this result set

**Results Key:**
**JNL** = Journal or Magazine   **CNF** = Conference   **STD** = Standard

**1 Advanced synchronous scan test methodology for multi clock domain ASICs**
*Schmid, J.; Knablein, J.;*

VLSI Test Symposium, 1999. Proceedings. 17th IEEE , 25-29 April 1999

Pages:106 - 113

[\[Abstract\]](#)
[\[PDF Full-Text \(248 KB\)\]](#)
**IEEE CNF**
**2 Scan test data volume reduction in multi-clocked designs with safe capture technique**
*Jain, V.; Waicukauski, J.;*

Test Conference, 2002. Proceedings. International , 7-10 Oct. 2002

Pages:148 - 153

[\[Abstract\]](#)
[\[PDF Full-Text \(439 KB\)\]](#)
**IEEE CNF**
**3 High-frequency, at-speed scan testing**
*Xijiang Lin; Press, R.; Rajski, J.; Reuter, P.; Rinderknecht, T.; Swanson, B.; Tamarapalli, N.;*

Design &amp; Test of Computers, IEEE , Volume: 20 , Issue: 5 , Sept.-Oct. 2003

Pages:17 - 25

[\[Abstract\]](#)
[\[PDF Full-Text \(292 KB\)\]](#)
**IEEE JNL**
**4 System issues in boundary-scan board test**
*Parker, K.P.;*

Test Conference, 2000. Proceedings. International , 3-5 Oct. 2000

Pages:724 - 728

[\[Abstract\]](#)
[\[PDF Full-Text \(308 KB\)\]](#)
**IEEE CNF**

---

**5 Test and debug techniques for multiple clock domain SoC devices***Youngblood, R.R.;*

Electronics Manufacturing Technology Symposium, 2004. IEEE/CPMT/SEMI 29 International , July 14-16, 2004

Pages:202 - 205

[\[Abstract\]](#) [\[PDF Full-Text \(500 KB\)\]](#) [IEEE CNF](#)

---

**6 Eliminating non-determinism during test of high-speed source synchronous differential buses***Mohanram, K.; Toubia, N.A.;*

VLSI Test Symposium, 2003. Proceedings. 21st , 27 April-1 May 2003

Pages:121 - 127

[\[Abstract\]](#) [\[PDF Full-Text \(347 KB\)\]](#) [IEEE CNF](#)

---

**7 Test and debug strategy of the PNX8525 Nexperia™ digital video platform system chip***Vermeulen, B.; Oostdijk, S.; Bouwman, F.;*

Test Conference, 2001. Proceedings. International , 30 Oct.-1 Nov. 2001

Pages:121 - 130

[\[Abstract\]](#) [\[PDF Full-Text \(877 KB\)\]](#) [IEEE CNF](#)

---

**8 A method for synchronizing IEEE 1149.1 test access port for chip level testability access***Bhavsar, D.;*

VLSI Design, 1998. Proceedings., 1998 Eleventh International Conference on Jan. 1998

Pages:289 - 292

[\[Abstract\]](#) [\[PDF Full-Text \(360 KB\)\]](#) [IEEE CNF](#)

---

**9 Test generation for designs with multiple clocks***Xijiang Lin; Thompson, R.;*

Design Automation Conference, 2003. Proceedings , 2-6 June 2003

Pages:662 - 667

[\[Abstract\]](#) [\[PDF Full-Text \(706 KB\)\]](#) [IEEE CNF](#)

---

**10 The testability features of the 3rd generation ColdFire<sup>(R)</sup> family of microprocessors***Crouch, A.L.; Mateja, M.; McLaurin, T.L.; Potter, J.C.; Tran, D.;*

Test Conference, 1999. Proceedings. International , 28-30 Sept. 1999

Pages:913 - 922

[\[Abstract\]](#) [\[PDF Full-Text \(800 KB\)\]](#) [IEEE CNF](#)

---

**11 Increasing the fault coverage in multiple clock domain systems by on-line testing of synchronizers***Petre, O.; Kerkhoff, H.G.;*

On-Line Testing Workshop, 2001. Proceedings. Seventh International , 9-11 J

2001  
Pages:95 - 99

[\[Abstract\]](#) [\[PDF Full-Text \(316 KB\)\]](#) [IEEE CNF](#)

---

**12 Wrapper design for testing IP cores with multiple clock domains**

*Qiang Xu; Nicolici, N.;*

Design, Automation and Test in Europe Conference and Exhibition, 2004.

Proceedings , Volume: 1 , 16-20 Feb. 2004

Pages:416 - 421 Vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(361 KB\)\]](#) [IEEE CNF](#)

---

**13 DFT timing design methodology for at-speed BIST**

*Sato, Y.; Sato, M.; Tsutsumida, K.; Kawashima, M.; Hatayama, K.; Nomoto, K.*

Design Automation Conference, 2003. Proceedings of the ASP-DAC 2003. Asia South Pacific , 21-24 Jan. 2003

Pages:763 - 768

[\[Abstract\]](#) [\[PDF Full-Text \(515 KB\)\]](#) [IEEE CNF](#)

---

**14 Design for test (DFT) for an embedded ARM system on a chip**

*Furlong, P.; Breathnach, D.; Daly, J.;*

Systems on a Chip (Ref. No. 1998/439), IEE Colloquium on , 5 Sept. 1998

Pages:4/1 - 411

[\[Abstract\]](#) [\[PDF Full-Text \(1556 KB\)\]](#) [IEEE CNF](#)

---

**15 Data invalidation analysis for scan-based debug on multiple-clock system chips**

*Goel, S.K.; Vermeulen, B.;*

European Test Workshop, 2002. Proceedings. The Seventh IEEE , 26-29 May 2002

Pages:61 - 66

[\[Abstract\]](#) [\[PDF Full-Text \(331 KB\)\]](#) [IEEE CNF](#)

---

[1](#) [2](#) [Next](#)

---

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved